PC SGRAM Specification

Revision 0.9

February 1998

Order Number: Not Applicable

Revision 0.9

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Revision History

Rev.	Description	Date
0.9	• Initial Industry Release	
0.8	• Initial Release for Internal Review	

1.0 Introduction

1.1 Objective

The objective of this document is to define a SGRAM specification (“PC SGRAM”). It should be easy to design and manufacture and highly cost optimized for the main stream volume desktop Graphics architecture PCs.

1.2 Scope of This Document

The scope of this document is limited to identify and define all the essential functionality that is needed to be implemented for “PC SGRAM”. Implementation details are left to the designers of the device.

1.3 Convention Used

- # sign after signals are used after the signal names for active low signals (e.g., CS#, RAS#, etc.)

2.0 Pinout

The pinout for 8Mb and 16Mb SGRAM configurations are shown below.

Figure 1. 256kx32 SGRAM Pinout

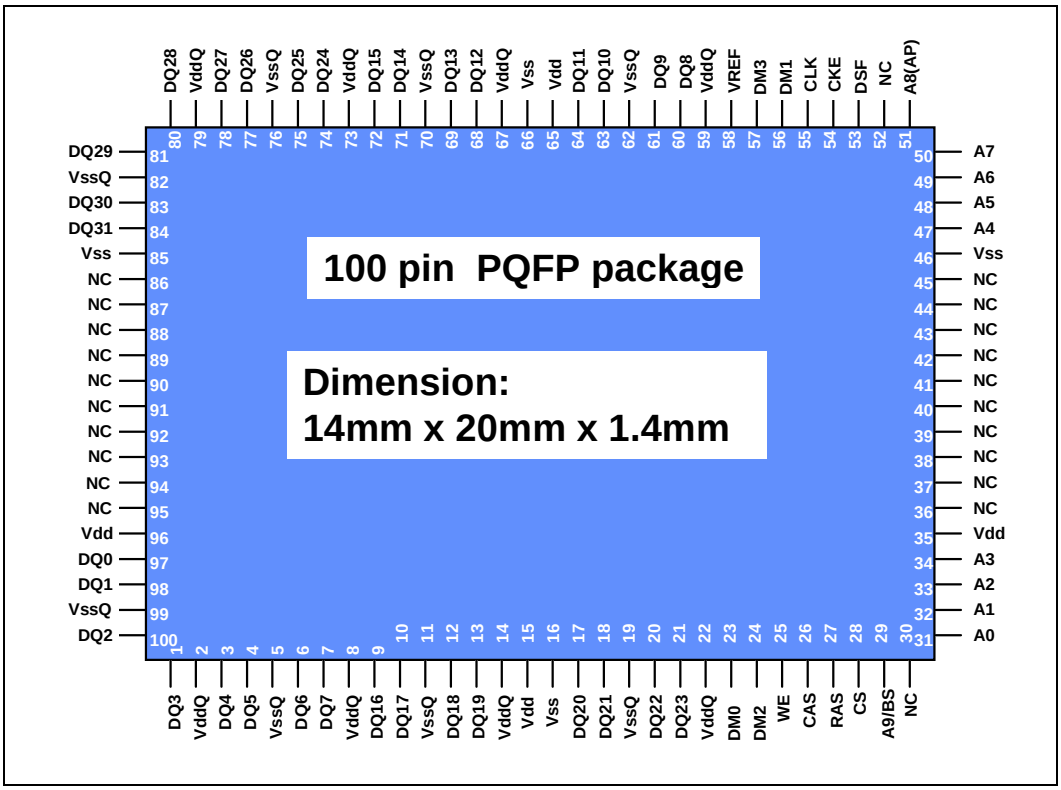
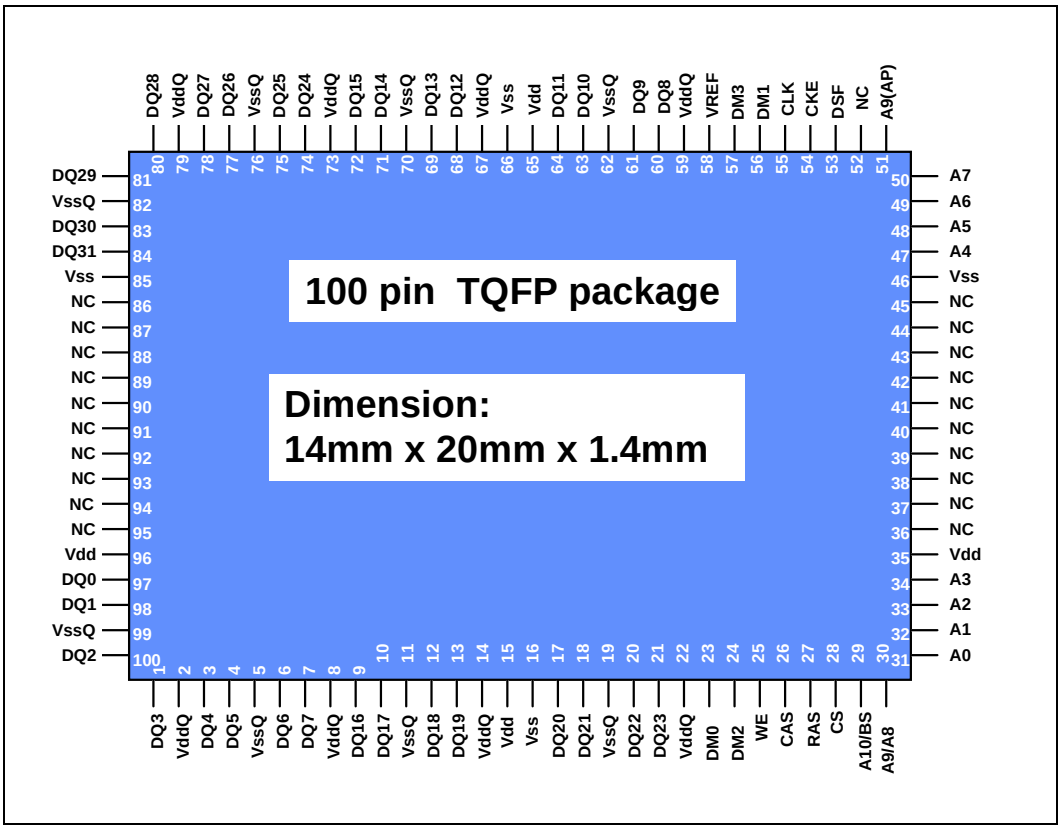


Figure 2. 512kx32 SGRAM Pinout



2.1 Pin Functional Descriptions (Simplified)

Table 1. Pin Functional Description

Symbol	Type	Description[a]
A[9:0]	Input - Synchronous	Address. Multiplexed Row and Column Address.
BA	Input - Synchronous	Bank Address. BA0 and BA1 specify the selected Bank during
AP	Input - Synchronous	Auto Precharge (Multiplexed with Row Address).
CLK	Input - Clock	Clock Input
CKE	Input - Clock Enable	Activates the CLK signal when high and deactivates when low. By deactivating the clock, CLKE low initiates the Power Down mode.
CS#	Input - Synchronous	Chip Select. Disables or enables the device operation by masking or enabling all inputs except CLK, CLK#, CKE, DQS, DQ and DM.
RAS#	Input - Synchronous	Row address strobe.
CAS#	Input - Synchronous	Column address strobe.
WE#	Input - Synchronous	Write Enable.
DQM[3:0]	Input	DQ Mask. Write data byte mask, Read output byte enables Active high. Read latency is two cycle from DQM and zero cycle for write. In write mode it masks the data from being written to the memory array. DM masking occurs in the same cycle during write operation. Write data byte mask, Read output byte enables. DQM is synchronous to the clock; thus, the masking occurs for the whole clock.
DQ[31:0]	Input/Output	Data IO pins.
DSF	Input - Synchronus	DFS: Enables the write per bit and Block write function. This pin has an internal pull-down resistor.
Vcc, Vss	Power pins	Supply Pins for the core
VccQ, VssQ	Power pins	Supply Pins for the output buffers

a. See the Truth Table and functional description for detailed information about the functionality

3.0 Control Registers

3.1 Mode Register and Modes Required to be Supported

PC SGRAM's mode register is accessed through the Mode Register Write command. The Mode Register is used to load the value of CAS Latency, Burst Type, & Burst Length

Table 2. Mode Register Description

Bit	Attribute	Description
BA	Reserved	Reserved: For normal operation, BA[1:0] should be "0"
A[9:7]	Reserved	Reserved: For normal operation, A[9:7] should be "000"
A[6:4]	WO	**CAS Latency:** 000 Reserved 001 Reserved 010 2 011 3 100 Reserved 101 Reserved 110 Reserved 111 Reserved
A[3:0]	WO	**Burst Type:** 0 = Sequential 1 = Interleave
A[2:0}	WO	**Burst Length:** **BT=0** **BT=1** 000 1 1 001 2 2 010 4 4 011 8 8 100 Reserved Reserved 101 Reserved Reserved 110 Reserved Reserved 111 Full Page Reserved

3.2 Special Mode Register

SGRAM's Special Mode Register is accessed through the Mode Register Write command. The Special Mode Register is used to load data into the Color Register or the Mask register. During the execution of the Special Mode Register Command, Bits A[6:5] determine if a new value is to be loaded into the Color and Mask registers.

Table 3. Special Mode Register

Bit	Attribute	Description
A[6]	WO	**Color Register:** 0 = Leave data unchanged for Color Register 1 = Load new data into Color Register
A[5:0]	Reserved	Reserved: For normal operation, these bits should always be "00000"

3.3 Color Register

Data is loaded into the Color Register through the Special Mode Register Write command. During the execution of the Special Mode Register Command, bit A[6] is used to determine if a new value is to be loaded into the Mask registers. If A[6] =1 during the special mode register command, then the value on DQ[31:0] is loaded into the Color Register. The color register supplies data for the block write command.

Table 4. Color Register

Bit	Default	Attribute	Description
31:0	00000000h	WO	**Color Register Data:** Data from these bits is used for Block Write Command.

4.0 Command Truth Table

Table 5. Command Truth Table

Function	Symbol	Command & Address								
		CS#	RAS#	CAS#	WE#	DSF	A8/ A9	DQM	A[7:0]	BA0, BA1
Mode Register Write	MRS	L	L	L	L	L	x	x	Data for Mode Register.	x
Special Mode Register Write	SMRWR	L	L	L	L	H	x	x	Data for SMR	x
CBR Refresh	CBR	L	L	L	H	L	x	x	x	x
Activate (Single Bank)	ACT	L	L	H	H	L	x	v	Row Address	Bank Address
Block Write	BLKWR	L	H	L	L	H	x	v	Column Address	Bank Address
Write	WRITE	L	H	L	L	L	x	v	Column Address	Bank Address
Write with Auto-precharge	WRITEAP	L	H	L	L	L	H	v	Column Address	Bank Address
Read	READ	L	H	L	H	L	L	x	Column Address	Bank Address
Read with Auto-precharge	READAP	L	H	L	H	L	H	x	Column Address	Bank Address
Burst Stop	BST	L	H	H	L	L	x	x	x	x
Precharge select Bank	PRE	L	L	H	L	L	L	x	x	Bank Address
Precharge All Banks	PALL	L	L	H	L	L	H	x	x	x
No Operation	NOP	L	H	H	H	L	x	x	x	x
Device Deselect	DSEL	H	x	x	x	x	x	x	x	x

Table 6. DQM Truth Table

Function	CKE n-1	CKE n	DQMx
Data write/output enable	H	X	L
Data mask/output disable	H	X	H
Byte x write mask	H	X	H

NOTE: H: High Level, L: Low Level, X: don't care, V: Valid data input

5.0 Operative Command Table

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
Idle	H	X	X	X	L	X	DSEL	Nop or Power Down	3
	L	H	H	H	L	X	NOP	Nop or Power Down	3
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	4
	L	H	L	L	L	BA,CA, A8/A9	WRITE/ WRITEAP	ILLEGAL	4
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	4
	L	L	H	H	L	BA,RA	ACT	Row Active	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	NOP	
	L	L	L	H	L	X	CBR/SELF	Refresh or Self refresh	5
	L	L	L	L	L	Op-code	MRS	Mode Register access	
	L	L	L	L	H	Op-code	SMRWR	Special Mode Register Write	
Row active	H	X	X	X	X	X	DSEL	NOP	
	L	H	H	H	L	X	NOP	NOP	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	Begin read: Optional AP	6
	L	H	L	L	L	BA,CA, A8/A9	WRITE/ WRITEAP	Begin write: Optional AP	6
	L	H	L	L	H	BA,CA	BLKWR	Begin Block write:	6
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4
	L	L	H	L	L	BA, A8/A9	PRE/PALL	Precharge	7
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	OP-code	MRS	ILLEGAL	14
	L	L	L	L	H	OP-code	SMRWR	ILLEGAL	14
READ	H	X	X	X	X	X	DSEL	Continue burst to end -> Row active	
	L	H	H	H	L	X	NOP	Continue burst to end -> Row active	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	Term burst, new read: Optional AP	8
	L	H	L	L	L	BA,CA, A8/A9	WRITE/ WRITEAP	Term burst, new wrtie: Optional AP	8,9
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	8,9
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
	L	L	H	L	L	BA,A8	PRE/PALL	Term burst, precharge	
	L	H	H	L	L	X	BST	Term burst	
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14
WRITE	H	x	x	x	x	X	DSEL	Continue burst to end ->Write recovering	
	L	H	H	H	L	X	NOP	Continue burst to end -> Write recovering	
	L	H	L	H	L	BA,CA,A 8/A9	READ/ READAP	Term burst, start read: optional AP	8,9
	L	H	L	L	L	BA,CA,A 8/A9	WRIT/ WRITEAP	Term burst, new write: optional AP	8
	L	H	H	L	L	X	BST	ILLEGAL	
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	8
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4
	L	L	H	L	L	BA, A8/A9	PRE/PALL	Term burst precharging	10
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Op Code	MRS	ILLEGAL	14
	L	L	L	L	H	Op Code	SMRWR	ILLEGAL	14
Read with auto precharge	H	X	X	X	X	X	DSEL	Continue burst to end -> precharging	
	L	H	H	H	L	X	NOP	Continue burst to end -> precharging	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	13
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14
Write with auto precharge	H	X	X	X	X	X	DSEL	Continue burst to end ->Write recovering with auto precharge	

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
	L	H	H	H	L	X	NOP	Continue bust to end-> Write recovering with auto precharge	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	13
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
	L	L	H	L	L	BA,A8	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14
Precharging	H	X	X	X	X	X	DSEL	NOP- Enter Idle after Trp	
	L	H	H	H	L	X	NOP	NOP-Enter Idle after Trp	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	4,13
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	4,13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	4,13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA,A8/ A9	PRE/PALL	NOP- Enter Idle after Trp	
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Op Code	MRS	ILLEGAL	14
	L	L	L	L	H	Op Code	SMRWR	ILLEGAL	14
Row activating	H	X	X	X	X	X	DSEL	NOP- Enter row active after Trcd	
	L	H	H	H	L	X	NOP	NOP- Enter row active after Trcd	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	4,13
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	4,13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	4,13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,11,13
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
Write Recovering	H	X	X	X	X	X	DSEL	NOP - Enter row active after Tdpl	
	L	H	H	H	L	X	NOP	NOP - Enter row active after Tdpl	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	Start Read, optional AP	9
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	New Write, optional AP	
	L	H	L	L	L	BA,CA	BLKWR	Block Write	
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	ILLEGAL	4,14
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Opcode	MRS	ILLEGAL	14
	L	L	L	L	H	Opcode	SMRWR	ILLEGAL	14
Write recovering with auto precharge	H	X	X	X	X	X	DSEL	NOP - Enter precharge after Tdpl	
	L	H	H	H	L	X	NOP	NOP - Enter precharge after Tdpl	
	L	H	L	H	L	BA,CA, A8/A9	READ/ READAP	ILLEGAL	4,9,13
Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
	L	H	L	L	L	BA,CA, A8/A9	WRIT/ WRITEAP	ILLEGAL	4,13
	L	H	L	L	H	BA,CA	BLKWR	ILLEGAL	4,13
	L	L	H	H	L	BA,RA	ACT	ILLEGAL	4,13
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	L	L	BA, A8/A9	PRE/PALL	ILLEGAL	4,14
	L	L	L	H	L	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	L	Op Code	MRS	ILLEGAL	14
	L	L	L	L	H	Op Code	SMRWR	ILLEGAL	14
Refreshing	H	X	X	X	X	X	DSEL	NOP - Enter idle after trc	
	L	H	H	H	L	X	NOP	NOP- Enter idle after trc	
	L	H	L	X	X	X	READ/ READAP	ILLEGAL	14
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	H	X	X	X	ACT/PRE/PALL	ILLEGAL	14
	L	L	L	X	X	X	CBR/SELF/ MRS	ILLEGAL	14

Table 7. Operative Command Table

Current state	CS#	RAS#	CAS#	WE#	DSF	Address	Command	Action	Notes
Mode Register accessing	H	X	X	X	X	X	DSEL	NOP - Enter idle after tmrd	
	L	H	H	H	L	X	NOP	NOP - Enter idle after tmrd	
	L	H	L	X	X	X	READ/ WRITE/ READAP/ WRITEAP/ BLKWR	ILLEGAL	14
	L	H	H	L	L	X	BST	ILLEGAL	
	L	L	X	X	X	X	ACT/PRE/ PALL/ CBR/ SELF/MRS/ SMRWR	ILLEGAL	14

NOTES:
1. H: High Level, L: Low Level, X: don't care, V: Valid data input, BA: Bank Address, AP: (Auto Precharge), CA: (Column Address), RA: (Row Address)
2. All entries assume that CKE was active (high level) during the preceding clock cycle.
3. If both banks are idle and CKE is inactive (low level), then in power down mode.
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
5. If both banks are idle and CKE is inactive (low level), then Self refresh mode.
6. Illegal if trcd is not satisfied.
7. Illegal if tras is not satisfied.
8. Must satisfy burst interupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy tdpl.
11. Illegal if trrd is not satisfied.
12. Burst Stop command is disabled.
13. Ilegal for single bank, but legal for other banks in multi-bank devices.
14. Illegal for all banks.

6.0 Row/Column Addressing Per Memory Size/# Banks

Table 8. Row, Column and Bank addressing

Parameter	2x128kx32 (8Mb)	2x256kx32 (16Mb)
Bank Address	BA	BA
Row Address	A[8:0]	A[9:0]
Column Address	A[7:0]	A[7:0]
Auto-Precharge	A8	A9
Page Size	256x32	256x32

7.0 Functional Description

7.1 Power Up Sequence

The SGRAM should be initialized by the following sequence of operations:

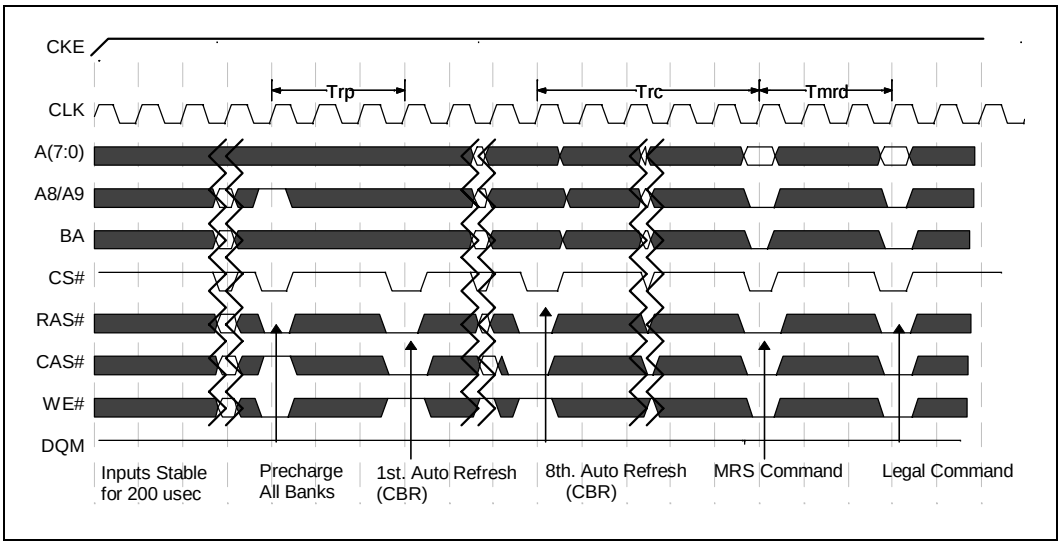
- Clock will be applied at power up along with power (clock frequency will be unknown).
- The clock will be stabilized within 100usec after power stabilizes.
- All the control inputs, RAS#, CAS#, WE#, CS# will be held in an undefined state during reset. After reset is complete RAS#, CAS#, WE#, and CS# will be held inactive before the first access to SGRAM is attempted.
- The levels on all the address inputs should be ignored. (All the addresses inputs can be indeterminate.)

Initialization Sequence

The initialization sequence can be issued at *anytime*. Following the initialization sequence, the device must be ready for full functionality. SGRAM devices are initialized by the following sequence:

- At least one NOP cycle will be issued after the 1msec device deselect.
- A minimum pause of 200usec will be provided after the NOP.
- A precharge all (PALL) will be issued to the SGRAM.
- 8 Auto refresh (CBR) refresh cycles will be provided.
- A mode register set (MRS) cycle will be issued to program the SGRAM parameters (e.g., Burst length, CAS# latency, etc.).
- After MRS, the device should be ready for full functionality within 3 clocks after T_{mrd} is met.

Figure 3. Power Up Initialization Sequence



7.2 Precharge Selected Bank

The precharge operation should be performed on the active bank when precharge selected bank command is issued. When the precharge command is issued with address A8/A9 low, BA selects the bank to be precharged. At the end of the precharge selected bank command the selected bank should be in idle state after the minimum T_{RP} is met.

7.3 Precharge All

All the banks should be precharged at the same time when this command is issued. When the precharge command is issued with address A8/A9 high, then all the banks will be precharged. At the end of the precharge all command all the banks should be in idle state after the minimum T_{RP} is met.

7.4 NOP and Device Deselect

The device should be deselected by deactivating the CS# signal. In this mode SGRAM should ignore all the control inputs. The SGRAM is put in NOP mode when CS# is active and by deactivating RAS#, CAS# and WE#. For both Deselect and NOP the device should finish the current operation when this command is issued.

7.5 Row activate

This command is used to select a row in a specified bank of the device. Read and write operations can only be initiated on this activated bank after the minimum T_{RCD} time is elapsed from the activate command.

7.6 Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating CS#, CAS# and de-asserting WE# at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

7.7 Write Bank

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating CS#, CAS# and WE# at the same clock sampling (rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

7.8 Block Write

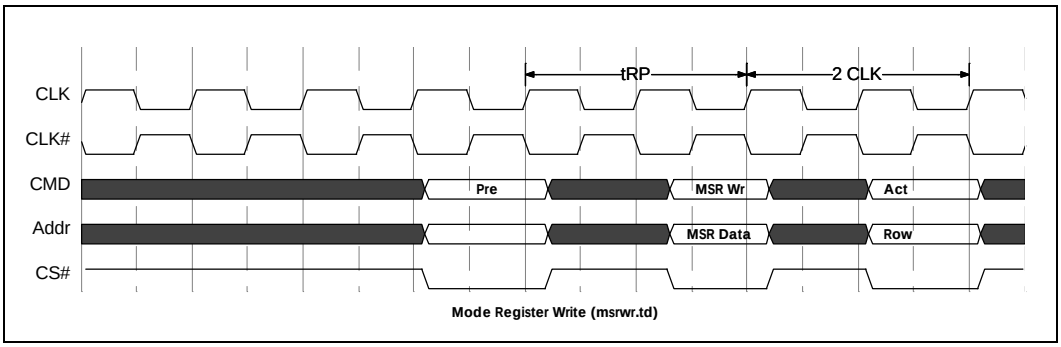
The Block Write command is used to write a block of data to an active row and bank within the device. The Block Write command is issued by driving CS# low, RAS# high, CAS# low, WE# low and DSF high. A Block Write command is a non-burst write command that writes data to 8 columns simultaneously. The data value contained in the Color Register (CR) is written to eight consecutive column locations addressed by A[7:3].

A Block Write access requires a minimum time of T_{BWC} to execute. No new commands can be executed until T_{WBC} is met except for Activate and Precharge command to the other banks.

7.9 Mode Register Set

This command is used to program the SGRAM for the desired operating mode. This command should be used after power up as defined in the power up sequence before the actual operation of the SGRAM is initiated. The functionality of the SGRAM device can be altered by re-programming the mode register through the execution of Mode Register Set command. All the banks should be precharged (i.e., in idle state) before the MRS command can be issued.

Figure 4. Mode Register Set Command

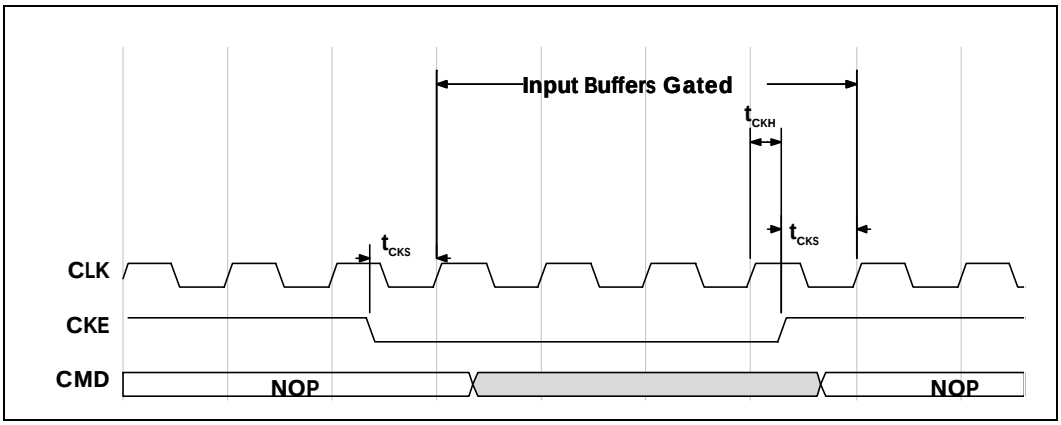


7.10 Power Down Mode

The Power down mode for PC SGRAM can be entered when both banks are in idle state (precharged) and CKE is asserted low. When in power down mode all input and output buffers are de-activated (except for CKE). If the device stays in the power down mode for more than 15.6 usec (refresh interval), then the PC SGRAM will loose data.

The power down mode can be exited by driving CKE high again. CKE assertion and de-assertion should meet the CKE setup and hold time (t_{CKS} and t_{CKH}).

Figure 5. Timing for Power Down Mode



8.0 Essential Functionality for the “PC SGRAM” device

The functionality that are essential for the “PC SGRAM” device are described below:

- Burst Read
- Burst Write
- Multi bank access
- Burst Read with Autoprecharge
- Burst Write with Autoprecharge
- Burst Read terminated with precharge
- Burst Write terminated with precharge
- Burst Read terminated with another Burst Read/Write
- Burst Write terminated with another Burst Write/Read
- DQM masking
- Fastest command to command delay of 1 clock
- Precharge All command
- Auto Refresh
- CL=2,3
- Burst Length 1,2, 4 & 8

8.1 Burst Read and Burst Write

Burst read and write commands are initiated as shown in the diagram below. The bank first needs to be activated (if not already activated) through the activate bank command and then the read or write command should be initiated. Read and write is distinguished by the WE# signal state as shown. T_{RCD} (RAS to CAS delay) must be met to initiate a command after the activate command.

8.2 Multi- bank ping pong access

Two bank ping pong access is described in the following diagram. Another bank can be activated while the first bank is being accessed as shown. RAS to RAS delay T_{RRD} must be met while activating another bank.

8.3 Read and Write with autoprecharge

Burst reads and writes with auto precharge commands are initiated *with autoprecharge if A8/A9 is to high* while the read or write commands are issued.

8.3.1 Precharge Command After a Burst Read

The earliest a precharge command can be issued after a Read command without the loss of data is CL + BL - 2 clocks. The precharge command can be issued as soon as the tras time is met. The earliest time that precharge can be issued is shown for the CAS Latency = 3 devices.

8.3.1.1 Precharge Termination of a Burst Read

Burst Read (with no autoprecharge) can be terminated earlier using a precharge command along with the DQM. This terminates reads when the remaining data elements are not needed. It allows starting the precharge early. The remaining data is undefined. DQM should be used to mask.

8.3.1.2 Precharge Command After a Burst Write

The earliest time that precharge can be issued is T_{DPL} clocks after the last data.

8.3.1.3 Precharge Termination of a Burst Write

To terminate Burst Write early with precharge command DQM signal should be used as shown. Data sampled T_{DPL} clocks before precharge command will be written correctly. Data sampled after and before the precharge command is undefined. DQM should be used to prevent the location from being corrupted.

8.3.2 Read Terminated By Read

A Read Command should terminate the previous read command and the data should be available after CAS Latency for the new command. Fastest command to command delay is determined by T_{CCD}

8.3.3 Write Terminated By Write

A Write Command should terminate the previous write command and the new burst write command should start with the new command as shown. Fastest command to command delay is determined by T_{CCD} .

8.3.4 Read Terminated By Write

A Write Command should terminate the previous read command and the new burst write should start. The DQM must be held active to keep the output buffer in HiZ as shown to prevent the internal IO buffer conflict between the read data (in pipe) and the write data driven on the input pins.

8.3.5 Write Terminated By Read

A Read Command should terminate the previous write command and the new burst read should start as shown. In case of with T_{CCD} =1, CL=3 and tdqz=2, there is no loss of data bandwidth even if DQM is activated to mask the write data.

In the case of CL=2 and tdqz=2, the activation of DQM signal causes the first read data to be lost, if read command is issued (T_{CCD} =1). To preserve the first read data the issue of READ command has to be delayed (T_{CCD}=2). This implementation reduces the command bus utilization.

If a Precharge-All command is detected by SGRAM component in CLK(n), then there will be no commands presented to this component until CLK(n+tRP).

bank command.

8.4 Back to Back Command Support

Minimum command to command delay of 1 Clock should be supported.

8.5 Auto Refresh (CBR) Command

An auto refresh (CBR) should be used to refresh the SGRAM array explicitly. Refresh addresses should be generated internally by the SGRAM device and incremented after each auto refresh automatically. No commands (including another auto refresh) should be issued until a minimum T_{RC} is satisfied.

9.0 SGRAM AC/DC Parameters

9.1 DC Specifications for 100-166 MHz

Table 9. Absolute Maximum D.C. Rating

Symbol	Parameter	Min	Max	Units	Notes
Vin, Vout	Voltage on any pin w.r.t V_{SS}	-0.5	V_{DD} + 0.5	V	
V_{DD}, V_{DDQ}	Voltage Supply pins pin w.r.t V_{SS}	-0.5	4.5	V	
Ts	Storage Temperature	-55	125	°C	

Table 10. D.C Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
VDD	Supply Voltage		3.135	3.6	V	
VDDQ	I/O Supply Voltage		3. 135	3.6	V	
Iil	Input Leakage Current	0 < Vin < VDDQ	-10	+10	µA	1,2
Cin	Input Pin Capacitance	@1MHz	2.5	5.0	pF	Target 3.75pf
CI/O	I/O Pin Capacitance	@1MHz	4.0	6.5	pF	Target 5.25pf
Cclk	Pin Capacitance	@1MHz	2.5	4.0	pF	Target 3.25pf
Lpin	Pin Inductance			10	nH	2
Ta	Ambient Temperature	No Airflow	0	65	°C	

NOTES:
1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

9.2 A.C. Specifications for 100-166 MHz

Table 11. Maximum AC Operating Requirements

Symbol	Parameter	Min	Max	Units	Notes
Vih	Input High Voltage	2.0	VDDQ+2.0	V	1,2
Vil	Input Low Voltage	VSSQ – 2.0	0.8	V	1,2

NOTES:
1. The overshoot and undershoot voltage duration is <=3ns with no input clamp diodes
2. The VDDQ and VSSQ are the operating parameters (not absolute max. parameters)

The refresh rate for all devices is assumed at a maximum of 15.6us per row per the table below.

Table 12. Refresh Rate

Symbol	Parameter	Min	Max	Units	Notes
Tref	Refresh rate / row	15.6		usec	1

NOTE:
1. The overall array refresh is determined by multiplying the specified row refresh rate by the number of rows in the total array.

9.3 A.C. Timing Parameters for 100-166 MHz

Table 13. 100, 125, 143MHz & 166MHz AC Timing Parameters

		100		125		143		166		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
Clock Period	t_{CK}		10		8		7		6	ns
CAS Latency	CL	2	3	2	3	2	3	2	3	CLK
CLK to valid output delay (max)	T_{AC} (max)		7		6		6		5.5	ns
Output data hold time	T_{OH}	2.5		2.5		2.5		2.5		ns
Address & Command Input setup time	T_{AS}	2.5		2.5		2		1		ns
Address & Command Input hold time	T_{AH}	1		1		1		1		ns
Data Input setup time	T_{DS}	2.5		2		1.5		1		ns
Data Input hold time	T_{DH}	1		1		1		1		ns
Activate to Activate Delay (Different bank)	T_{RRD}	2		2		2		2		CLK
Read to Read Command Delay,Write to Write Command Delay	T_{CCD}	1		1		1		1		CLK
Activate to Read, Write or Block Write Delay	T_{RCD}	2		3		3		3		CLK
Precharge to Activate Delay (single bank precharge)	T_{RP}	2		3		3		3		CLK
Activate to Precharge Delay	T_{RAS}	5		6		7		7		CLK
Activat to Activate Delay (Same Bank), Refresh Cycle time	T_{RC}	7		9		10		11		CLK
Block Write to Precharge Delay	T_{BPL}	2		2		2		2		CLK
Block Write Cycle Time	T_{BWC}	2		2		2		2		CLK
Last write data in to precharge	T_{DPL}	1		1		1		1		CLK

NOTE:
1. Output I/O Timings measured with a 30pf load

9.4 DC Specifications for 166-250 MHz

Absolute Maximum D.C. Rating (TBD)

D.C Operating Requirements (TBD)

9.5 A.C. Specifications for 166-250 MHz

Maximum AC Operating Requirements (TBD)

Refresh Rate (TBD)

9.6 A.C. Timing Parameters for 166-250 MHz

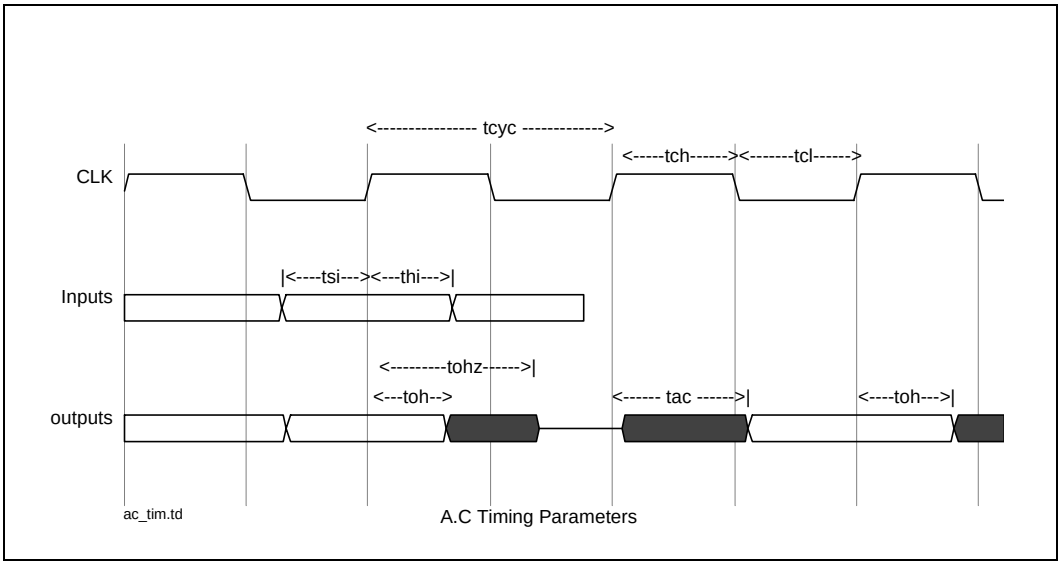
Table 14. 166, 200, 250 MHz & 166 MHz AC Timing Parameters

		166		200		250		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Period	t_{CK}	6		5		4		ns
CAS Latency	CL	2	3	2	3	2	3	CLK
CLK to valid output delay (max)	T_{AC} (max)		5.5	TBD		TBD		ns
Output data hold time	T_{OH}	2.5		TBD		TBD		ns
Address & Command Input setup time	T_{AS}	1		TBD		TBD		ns
Address & Command Input hold time	T_{AH}	1		TBD		TBD		ns
Data Input setup time	T_{DS}	1		TBD		TBD		ns
Data Input hold time	T_{DH}	1		TBD		TBD		ns
Activate to Activate Delay (Different bank)	T_{RRD}	2		TBD		TBD		CLK
Read to Read Command Delay,Write to Write Command Delay	T_{CCD}	2		TBD		TBD		CLK
Activate to Read, Write or Block Write Delay	T_{RCD}	3		TBD		TBD		CLK
Precharge to Activate Delay (single bank precharge)	T_{RP}	3		TBD		TBD		CLK
Activate to Precharge Delay	T_{RAS}	7		TBD		TBD		CLK
Activat to Activate Delay (Same Bank), Refresh Cycle time	T_{RC}	11		TBD		TBD		CLK
Block Write to Precharge Delay	T_{BPL}	2		TBD		TBD		CLK
Block Write Cycle Time	T_{BWC}	2		TBD		TBD		CLK
Last write data in to precharge	T_{DPL}	2		TBD		TBD		CLK

9.7 IBIS: I/V Characteristics for Input and Output Buffers

(TBD)

Figure 6. A.C Timing Parameters



NOTE:
1. Reference level is set at 1.5V, AC measurements are specified into 50pf load.
2. input edge rates are specified as 1.0v/ns minimum (0.8v to 2.0v)

9.8 IBIS Reference

The IBIS Open Forum is an industry-wide forum that controls the official IBIS specification. Minutes of IBIS meetings, email correspondence, proposals for specification changes, etc. are on-line at "vhdl.org". To join in the email discussions, send a message to "ibis-request@vhdl.org" and request that your name be added to the IBIS mail reflector. Be sure to include your email address.

To download a copy of the specification, the golden parser, various public-domain models, the *IBIS Overview* in PostScript, and other information, either phone in by modem or use FTP.

FTP:	(IP address 198.31.14.3) login as "anonymous" password is your email address
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IBIS-related files are in the directory "/pub/ibis" and its sub-directories.

To get documents by email, send an email message to "archive@vhdl.org" with the following commands in the message body:

path <your_email_address>
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For direct modem access, dial-up to the vhdl.org system at (408) 945-4170. You can use any baud rate up to 14,400, any parity, start and stop bits, and any v.* settings. Log in using the "guest" account. Simple UNIX commands such as "cd", "ls", and "cat" are available and you can download files using "kermit", "zmodem", or "sz" (another zmodem application).

For Internet access, use "ftp vhdl.org" (or "ftp 198.31.14.3") and log in as user "anonymous". The gopher utility is available and highly recommended. Gopher to "vhdl.org". Set "binary" mode for transferring binary files (*.doc, *.fm, *.xls).

The IBIS home page can be found at **http://www.eia.org/eig/ibis/ibis.htm**